REMARKS

Claims 1-25 remain in this application. Claim 7 has been amended to overcome the objection of the Examiner. Claims 2, 4, 11, 20, and 22 have been amended to put claims into allowable form. Claims 6 and 10 have been amended to put them into better form. The Office Action indicates that claims 2-6, 11-18 and 20-25 would be allowable if put into independent format. These claims should be properly allowed in view of the amendments.

OBJECTIONS TO THE CLAIMS

Claim 7 was objected to in that the Office Action states that the limitation cited in claim 7 is already claimed in claim 1(a). Claim 7 has been amended to more expressly recite limitations and differentiate it from claim 1. Accordingly, reconsideration and withdrawal of the objection to claim 7 is respectfully requested.

REJECTIONS TO THE CLAIMS UNDER 35 U.S.C. § 103(a)

Claims 1, 7-10, and 19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,438,501 to Weber ("Weber") in view of U.S. Patent No. 5,481,568 to Yada ("Yada").

Claim 1, for example, recites a method where over-sampled data is received and a sample bit is detected along with bits on either side of it having an opposite value. The sample bit is output with the data in an inverted form to correct for an error (e.g., a glitch). Similar limitations are found in independent claims 7 and 19.

The device of Weber is designed to create a pseudorandom binary sequence. Looking at Fig. 1, an 18-stage shift register 100 is provided that outputs the 14th and 17th stages to an XOR gate 135 (see Col. 2, lines 28-41). An early access point to the shift registers is also retrieved as an output signal 102 (see Col. 3, lines 1-11). Whenever signal 102 is low, the inverter 130 outputs a logic "1" value, which is input to XOR gate 140 causing this gate to act as an inverter. Accordingly, the output of XOR gate 135 is negated and provided as a data input to the shift register. Aside from the receipt of over-sampled data, claim 1 recites detecting a sample bit having one logic value and, on either side of it, bits having an opposite logic value and outputting "the received word" with the one logic value inverted. The Office Action makes no attempt at identifying one example of a sample bit having one logic value in Weber as recited in the claim. If the 14th and 17th stage outputs are different from one another and the earliest stage output is a logic "0", then the data input for the shift register will be a logic "0." If these two values are the same, then the data input will be a logic "1" when the earliest stage output is a logic "0." When the earliest stage output is a logic "1," then the data input from the shift register will be the XOR of the 14th and 17th stages (i.e., "1" if they're different, "0" if they're not).

Yada fails to make up for the deficiencies of Weber. Yada refers to a data detecting apparatus using over sampling as an interpolation means. Over-sampled data, such as shown in Fig. 2b is fed to an interpolating filter 11. An example of the output signal from filter 11 is shown in Fig. 2(d). Yada does not refer at all to detecting a sample bit in received over-sampled data as having one logic value and bits on either side of the sample bit having an opposite logic value. Yada does not refer to outputing a received word with the sample bit having the one logic value inverted. At best, Yada only provides the disclosure of over-sampling, a concept well-known in

the art. The present invention pertains to a method and apparatus of filtering such data. Features of the claims are wholly missing from Yada. Moreover, there is absolutely no suggestion in these references as to how they would be combined. Weber refers to a shift register that outputs pseudorandom values. There is no over-sampling needed in Weber, and thus no need for the apparatus of Yada..

Since features of the claims are missing from and not suggested by the Weber and Yada reference, taken singularly or in combination, reconsideration and withdrawal of the rejection of claims 1, 7-10 and 19 under 35 U.S.C. § 103(a) is respectfully requested.

CONCLUSION

For all the above reasons, the Applicant respectfully submits that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (202) 220-4200 to discuss any matter concerning this application. The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. § 1.16 or § 1.17 to Deposit Account No. 11-0600.

Respectfully submitted,
KENYON & KENYON

Dated: September 7, 2004 By: _____
Shawn W. O'Dowd
Reg. No. 34,687

KENYON & KENYON
1500 K Street, NW
Suite 700
Washington, DC 20005
(202) 220-4200 telephone
(202) 220-4201 facsimile
DC-504316

DC01 504316 v 1